S/N 08/984,560

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Jeffrey S. Mailloux et al.	Examiner:	Hong Kim
Serial No.:	08/984,560	Group Art Unit:	2751
Filed:	December 3, 1997	Docket:	303.623US2
Title:	MEMORY DEVICE WITH PATTERNED AND PATTERNLESS ADDRESSING		

AMENDMENT & RESPONSE UNDER 37 C.F.R. § 1.116

Box AF
Assistant Commissioner for Patents
Washington, D.C. 20231

In response to the final Office Action mailed March 17, 2000, please amend the application as follows:

IN THE CLAIMS

Please amend the claims as follows:

15. (Once Amended) A storage device, as in Claim 14, further compr[om]ising a counter coupled for receiving a selected portion of the external address for generating an internal address.

59. (Once Amended) A memory device, comprising:

a memory array;

control logic operatively connected to the memory array, the control logic for selecting between [a] an unpatterned pipeline and a patterned burst data pattern for accessing the memory array; and

switching circuitry for switching between a first pathway and a second pathway depending on which of said pipeline scheme and said burst scheme is selected.